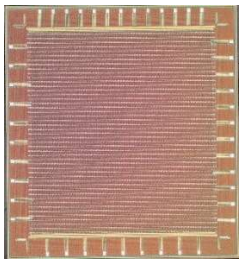
Free and Open Chip Design Tools

Emergence, Productive Use, Options for Actions

A Working Paper for Designers, Investors, Managers, Governments, and the Interested Public

*By Arnd Weber, Norbert Herfurth, and Steffen Reith**



ASIC chip, created with open design tools, manufactured by IHP Frankfurt (Oder), Germany

"With open EDA, we can create tailored microchips for satellite electronics, just like Apple designs custom chips"
Thomas Parry, SPHERICAL, Rotterdam

"Currently, we have to buy crypto algorithms under closed source"
Torsten Grawunder, Swissbit Germany

"Our open-source tool DreamPlace has been used in the design flows at Google and Nvidia"
Yibo Lin, Peking University

"The trajectory of open-source EDA is unstoppable and irreversible"
Andrew Kahng, UC San Diego

*Arnd Weber is a German consultant, Norbert Herfurth works for IHP – Leibniz Institute for High Performance Microelectronics, Germany, and Steffen Reith is with RheinMain University of Applied Sciences, Germany. In 2020, the authors started to lobby for the public funding of open-source Electronic Design Automation (EDA) and a Process Design Kit (PDK) for the creation of application-specific integrated circuits (ASICs) in Germany.

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Introduction

Designing semiconductor chips is usually expensive, as the proprietary software to perform it is essentially in the hands of just three large companies. Using a fabrication plant for the physical production is expensive, too. Yet there is a new approach emerging for this design, using free and open tools and components to reduce the costs and allow new users to participate in chip design. Even for existing companies which already design chips the new approach has the potential to be cheaper, and they can participate in the design and further the development of the tools. Companies which so far have been prevented from designing their own chips due to these barriers to entry can now create innovative products. Even young people can explore how to design a chip and obtain a working physical device at low cost.

This paper aims to provide an overview of this new approach to design, the opportunities it offers, the options available to improve it, and to describe how to participate in its development as well as how to benefit from it.

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In the next section, we provide a summary of our arguments. In the main section, the topic, past development events, and options for action are described in greater detail.

The latest version of this document is available at hep-alliance.org.

Summary

Overview

How can innovation in information technology (IT) be made easier? This is a question that is of particular relevance for the semiconductor industry, where chip designers in both business and academia face high barriers to entry. These are due in part to the stranglehold that a few large companies have over the design process. A strenuous effort is now being made to reduce these barriers; the potential reward is a flowering of innovative activity that could generate more advances at a lower cost in a field which still offers huge opportunities for creative ideas. Examples of these new processes include:

- Microchips tailored for specific industrial needs can be designed with open tools for a lower cost base, as is being done by the satellite avionics provider SPHERICAL. With the use of open-source tools, smaller companies can co-design system-level hardware and software without having to use the same expensive, proprietary tools as large, established companies.
- Development of open tool chains and fabrication processes, including electronic design automation (EDA) tools, which cannot be limited by embargoes, as the Chinese iEDA initiative demonstrates.
- Development of tools which are as usable as their closed-source proprietary equivalents, and sometimes even more efficient, e.g. Verilator for simulating a circuit and DREAMPlace for optimising the timing inside a chip. These tools have been developed by Google, Nvidia, NXP, and others, and are actively used for commercial product development in place of expensive proprietary alternatives. Their efficiency came about through international, open cooperation.
- Low-cost development of small, proof-of-concept chips as has already been enabled by the Tiny Tapeout project for more than thousand students worldwide, and a similar initiative in China called *One Student One Chip.*
- Integration of cryptographic components which are open and mathematically proven to work correctly, e.g. following the Caliptra standard, as targeted by the HEP-Alliance set up by the authors of this paper and supported by the German federal government.

Free and open EDA tools can support the full product development process, from the birth of an idea for a device with a custom semiconductor inside to sending the design required to produce a chip to a semiconductor fabrication site (fab). The term “open EDA” may relate to using open tools only for certain steps of the production process, such as simulating a chip, or for using it for the entire process from designing the chip up to the creation of all data to be sent to a fab. The latter may be done using proprietary Process Design Kits (PDKs), which typically require the user to sign a non-disclosure agreement (NDA), or one of the emerging open PDKs. These open PDKs, which do not require the user to sign an NDA, have been made available by SkyWater, GlobalFoundries, ICSprout, and IHP for relatively large, somewhat older “process nodes,” such as the well-established 130 nm node, which are still used for producing chips used in the automotive industry, armed forces, etc. The term

“node” here refers to the sizes of structures manufactured on the chip. Chinese semiconductor manufacturer ICSprout reportedly offers 55 nm production on 12-inch wafers (Zhao et al. 2025).

Historically the design of chips, and in particular application-specific chips (ASICs), has been expensive, with costs running into the millions. This is partially because developing the software to create properly working semiconductors is itself expensive. Such software has been said to be as valuable as gold because it is designed to lead to perfectly working chips with no unwanted internal interference, defects, or other design errors. For small companies or students, however, this software is difficult to use on devices like laptop computers and requires the signing of typically restrictive NDA and end-user licence agreements (EULAs) which do not allow the discussion of its pros and cons. The providers of these proprietary tools have been said to operate an oligopoly; thus enthusiasts, students, universities, armed forces, etc. have long been looking for software which is accessible to and usable by anybody. Governments have been supporting this endeavour, too, with initiatives ongoing in the US, in China, Germany, and elsewhere.

Advocates of open-source EDA sometimes argue that these tools will become as relevant as other open software like the Linux kernel, Apache web server, and more. However, there are three issues with this. Firstly, the development of ASICs with open EDA tools is costly and time-consuming, as it takes months and considerable money to have working proofs prepared and thus demonstrate the correctness of the tool. As a result some development efforts started with tools for freely programming field programmable gate arrays (FPGAs), off-the-shelf chips which can receive “gateware” to act in an application-specific manner but which, however, are typically more power-consuming and pricier than ASICs. Secondly, open EDA tools for ASIC production may require the use of a proprietary PDK, with its NDA and EULA, in order to access most modern chip production nodes. Thirdly, a commercial user may prefer to use a proprietary solution, as this reduces the risk of obtaining non-working ASICs costing millions. So history may not simply repeat itself: while you can use Linux instead of Microsoft Windows on your computer today, you may never get open access to the most modern semiconductor fabrication equipment as produced by companies like Durch ASML and run by Taiwanese TSMC.

So what does this mean? Some companies, as mentioned above, use selected free and open tools for developing or testing an innovation. Beyond that, additional open PDKs may or may not emerge. The likelihood of this increases if competition forces a fab to open its process or if governments fund the opening of a PDK.

What does this mean for investors? Companies which are used to designing chips can explore the new open approach, as Google, Nvidia, and many others already do, which can lead to more efficient or innovative designs. The costs of doing this can be shared throughout the industry, including Chinese players, as has been demonstrated by the RISC-V processor design community or the CHIPS Alliance.

For governments this provides the opportunity to support research on completely open processes, analogue designs for radio and other signal workloads, smaller process nodes, etc., to make the open approach more capable and more universally usable while enabling technological sovereignty.

In the next sections of this summary, we provide examples of existing and emerging commercial use of free and open tools, systems, and chip designs. The reader will see that we observed many developments in statu nascendi.

Illustrations of Existing Commercial Use

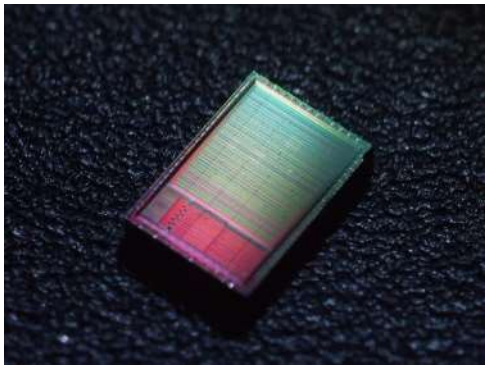


Figure 1: An ASIC produced with the open SkyWater fab process design kit and the OpenROAD toolchain (supported by Google and the US DARPA, resp.; Venn 2024/Tiny Tapeout, Spain). Efabless charged 10,000 USD for 100 chips of 10mm2, more than 1,000 students participated.

Figure 2: A Renesas, Japan, field programmable (FPGA) board to be used with the open, free Yosys synthesis tool which was developed in Austria (Wolf, Glaser 2013; Renesas 2025).

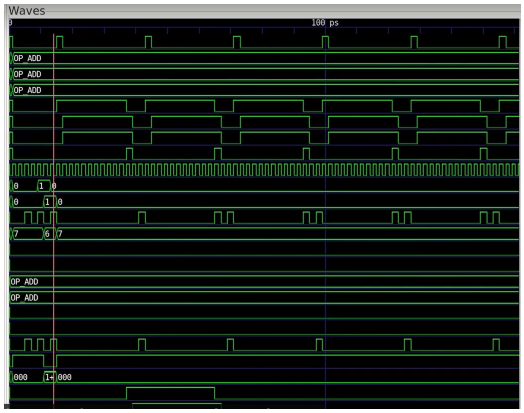


Figure 3: Verilator, an open-source simulator tool in some instances faster than commercial tools, showing here a representation of signals over time. Used by NXP, Tesla, Shunyao, and others (screenshot from BitByte 2024).

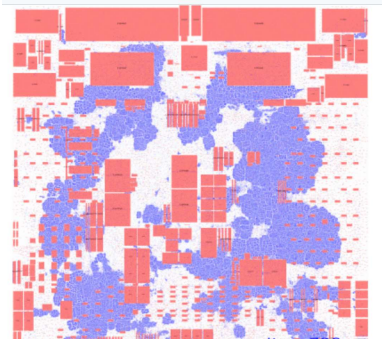


Figure 4: Open chip layout tool DREAMPlace 4.0 from China with origins in the US. Used to optimise timing in designs by Google, Nvidia, and others (DREAMPlace 2025).

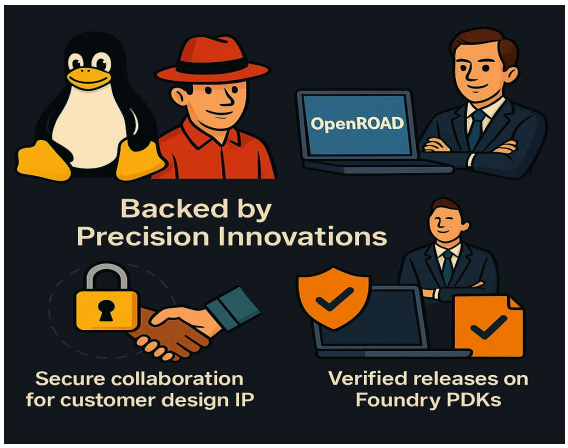


Figure 5: Services for the OpenROAD toolchain provided by the US company Precision Innovations, used, e.g. by Google for optimising designs (Kahng 2025).

Illustrations of Emerging Commercial Use

Figure 6: Prototypical security module from German IHP and partners, produced with the US OpenLane toolchain and the open VexRiscv processor design from Switzerland. It is designed to contain no Trojans by applying openness and mathematical proofs; to be updated to follow the Caliptra standard; with support from IAV and Swissbit (Henkes et al. 2024, Papon 2024; IHP 2024).

Figure 7: Prototype of an automotive Electronic Control Unit (ECU), to replace several other ECUs, designed with open tools (British/Spanish ChipFlow 2025a).

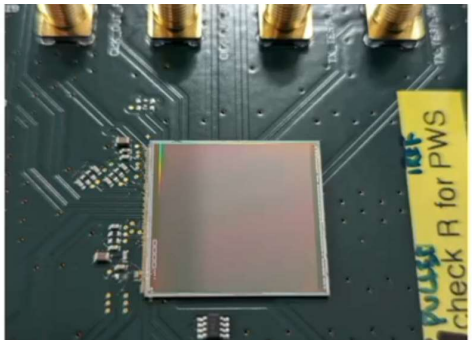


Figure 8: 10 Gbit/s serial data link prototype chip designed by Swiss company Dectris, with open EDA digital tools, to be fast, transparent, and cost-efficient (Hemperek 2024).

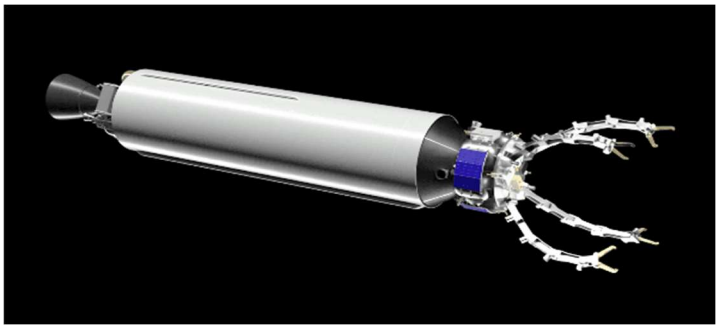


Figure 9: Optimised semiconductor design for a component in a HADES spacecraft, designed to be radiation-hardened and power-efficient, with hard- and software co-design using the open EDA tools Xschem, KLayout, Xyce, OpenLane, and Iverilog (British SPHERICAL 2025, Parry 2025a).

Figure 10: A gaming console, similar to the Trimui console pictured, to be designed with open Chinese iEDA with an open 55 nm PDK, by 2027 (Zhao et al. 2025). Already more than 1,200 students have been designing RISC-V processors (One Student One Chip).

Main Section

Challenges

The process of designing semiconductor chips is traditionally expensive, shielded by NDAs, and not accessible to companies with small-sized production batches. The proprietary software and hardware used may even be subject to export restrictions, such as ASML's lithography machines or essential EDA tools (cf. BBC 2023 and Financial Times 2025). Closed-source tools, meanwhile, could contain Trojan horses, as even the US Air Force worries (Coleman 2023). Such tools do not support a path towards sovereignty for countries working towards technological independence.

At the same time that closed equipment is very well suited for designing chips with the smallest structures and capable of operating with low energy consumption, e.g. by using extreme ultraviolet light (EUV) lithographic equipment available in the most recent semiconductor fabrication plants (cf. Fig. 11 and 12). Highly sophisticated software is needed to produce such small structures, which in turn means that development costs are high and the process is time-consuming (Olofsson 2018). As the costs are in the range of millions of US Dollars or Euros per design, and as NDAs need to be signed and restrictive EULAs observed, there is a shortage of students willing to learn how to use these tools as they cannot simply install them on their laptop computers, play around with them, or compare such proprietary software to emerging open chip design tools. NDAs and EULAs even prevent open comparison between different vendors' proprietary software and also against open-source tools.

Figure 11: A German Zeiss lens for an ASML EUV lithography machine (Zeiss 2025)

On one hand, this situation is beneficial for those companies which have the competence to develop chip design tools such as Cadence which, in 2023, had a revenue of around four billion US Dollars and made a profit of around one billion US Dollars (Wikipedia 2024). The industry's other major players are Synopsys and Siemens EDA (formerly known as Mentor Graphics), which form the so-called "Big Three." As PwC put it: "This oligopolistic structure complicates access to these essential EDA tools, especially for small and medium-sized enterprises." (PwC 2023). This situation led individuals and companies to search for better and cheaper solutions.

Figure 12: Slide illustrating how the Dutch ASML depends on research at the Belgian imec and inputs from many other countries, e.g. from Japanese Toppan (Pradeep 2022) and unmentioned ones like the German Trumpf Hüttinger plasma generators.

The Emergence of Open Chip Design

Enthusiasts, academics, and companies are developing free and open chip designs and related tools which have already begun to be used to produce ASICs. Designs and tools include processor designs like RISC-V, EDA tools to design circuits, and fab-specific PDKs to develop a physically producible implementation of a design, i.e. the production data to be sent to a semiconductor fabrication facility. With such open and free tools it is now possible to generate complete chip designs.

Excursus on RISC-V Processor Designs

In this paper we do not review developments such as the creation of RISC-V processors, of which billions have reportedly been integrated into the products of Western Digital, Google, Nvidia, and many others (HPCWire 2024). For example, the award-winning VexRiscv, which the authors use in their research projects, has been integrated by Efinix into their FPGA chips. Nor do we mention other developments such as root of trust elements, a field in which we are active, too, in order to keep the paper short and focused on EDA and hardware production (cf. Weber et al. 2018 and IHP 2024).

Logic of Open EDA

Open EDA tools were initially created by individuals who wanted to design chips freely without significant upfront costs and without signing NDAs which restrict open communication. Examples include Yosys for creating lists of components and their connections (Wolf, Glaser 2013), the Magic layout tool, and KLayout for viewing layout masks; work on the latter started in 2006 (Köfferlein 2022). Note that while there are sometimes key enthusiasts triggering the creation of an open tool, there are typically many partners involved in its ongoing development (cf. Fig. 13).

This open approach is similar to that of free and open software, such as the Linux operating system kernel or the Apache web server software. Many chip designs for processors, microcontrollers, and application-specific chips, as well as the ASIC design tools with which they were made, are free, open, and require no NDA to be signed. Any user can make changes quickly and directly, request changes from the creator of a component, or commission third parties to make changes on their behalf. It has been shown that such changes are typically implemented quickly and efficiently by the development community.

A key role in this proliferation was played by the US DARPA (Olofsson 2018), which led to the development of the OpenROAD toolchain. Google cooperated with the US SkyWater fab to provide an open PDK, and these two components allowed for a fully open process right up to the production of the file to be sent to the fab (Euphrosine 2022). Note that SkyWater is a "Trusted Foundry" which can offer long-running supplies of chips for the armed forces (Digitimes Asia 2023, U.S. Department of Commerce 2024). We mention this because possibly more fabs in other countries will be able to play a role in the long-running supply of chips and in open design.

Foundry-specific data from a PDK can be added in where needed. Furthermore, users can mix and match open tools with proprietary software where required for certain functionality. With the new, open approach, electronic design automation software can be made usable in a browser, users can create interfaces into artificial intelligence tools, and more. Hundreds of skilful developers are already working to improve open EDA software. For example, the OpenROAD toolchain has been used to design chips with node sizes of 12 nm, and Chinese tools have reportedly been used down to 28 nm – both reaching production using proprietary PDKs (Kahng 2023, Li 2024b). The company Precision Innovations is providing services for using and improving OpenROAD which are used by various companies such as Google (Kahng 2025). Note that many open EDA tools and results can be integrated into proprietary tools, as a permissive BSD-3 licence is used.

As the Communications of the ACM put it: "Electronic hardware design is no stranger to free and open source software, such as the SPICE (Simulation Program with Integrated Circuit Emphasis) analog simulator put into the public domain by researchers at the University of California at Berkeley in the early 1970s. Yet most users will access SPICE through proprietary tools that have each extended the engine in different ways." (2022)

Ahmed El-Mahmoudy, David Addison, Tariq B. Ahmad, Nikana Anastasiadis, Hans Van Antwerpen, Vasu Arasanipalai, Jens Arm, Sharad Bagri, Andrew Bardsley, Matthew Barr, Geoff Barrett, Julius Baxter, Jeremy Bennett, Michael Berman, Victor Besyakov, David Binderman, Johan Bjork, David Black, Tymoteusz Blazejczyk, Daniel Bone, Gregg Bouchard, Christopher Boumenot, Nick Bowler, Byron Bradley, Bryan Brady, Charlie Brej, J Briquet, Lane Brooks, John Brownlee, Jeff Bush, Lawrence Butcher, Ted Campbell, Chris Candler, Lauren Carlson, Donal Casey, Sebastien Van Cauwenberghe, Terry Chen, Enzo Chi, Robert A. Clark, Allan Cochrane, John Coiner, Laurens van Dam, Gunter Dannoritzer, Ashutosh Das, Bernard Deadman, John Demme, Mike Denio, John Deroo, Philip Derrick, Joe DErrico, John Dickol, Ruben Diez, Danny Ding, Ivan Djordjevic, Jonathon Donaldson, Sebastian Dressler, Alex Duller, Jeff Dutton, Usuario Eda, Chandan Egbert, Joe Eiler, Ahmed El-Mahmoudy, Trevor Elbourne, Robert Farrell, Eugen Fekete, Fabrizio Ferrandi, Brian Flachs, Andrea Foletto, Bob Fredieu, Duane Galbi, Christian Gelinek, Glen Gibb, Shankar Giri, Dan Gisselquist, Sam Gladstone, Amir Gonnen, Chitlesh Goorah, Xuan Guo, Neil Hamilton, Jannis Harder, Junji Hashimoto, Thomas Hawkins, Robert Henry, David Hewson, Jamey Hicks, Joel Holdsworth, Hiroki Honda, Alex Hornung, David Horton, Jae Hossell, Alan Hunter, James Hutchinson, Jamie Iles, Ben Jackson, Shareef Jalloq, Krzysztof Jankowski, HyungKi Jeong, Iztok Jeras, James Johnson, Christophe Joly, Franck Jullien, James Jung, Mike Kagen, Arthur Kahlich, Kaalia Kahn, Guy-Armand Kamendje, Vasu Kandadi, Patricio Kaplan, Ralf Karge, Dan Katz, Sol Katzman, Jonathan Kimmitt, Olof Kindgren, Dan Kirkham, Sobhan Klnv, Gernot Koch, Soon Koh, Steve Kolecki, Brett Koonce, Wojciech Koszek, Varun Koyyalagunta, David Kravitz, Roland Kruse, Sergey Kvachonok, Ed Lander, Steve Lang, Stephane Laurent, Walter Lavino, Christian Leber, Igor Lesik, John Li, Eivind Liland, Yu Sheng Lin, Charlie Lind, Andrew Ling, Paul Liu, Derek Lockhart, Arthur Low, Stefan Ludwig, Dan Lussier, Fred Ma, Duraid Madina, Julien Margetts, Mark Marshall, Alfonso Martinez, Yves Mathieu, Patrick Maupin, Jason McMullan, Elliot Mednick, Wim Michiels, Miodrag Milanovic, Wai Sum Mong, Sean Moore, Dennis Muhlestein, John Murphy, Richard Myers, Dimitris Nalbantis, Bob Newgard, Cong Van Nguyen, Paul Nitza, Pete Nixon, Lisa Noack, Mark Nodine, Andreas Olofsson, James Pallister, Brad Parker, Maciej Piechotka, David Pierce, Dominic Plunkett, David Poole, Mike Popoloski, Rich Porter, Niranjan Prabhu, Usha Priyadharshini, Mark Jackson Pulver, Prateek Puri, Marshal Qiao, Chris Randall, Anton Rapp, Josh Redford, Odd Magne Reitan, Frederic Requin, Alberto Del Rio, Oleg Rodionov, Paul Rolfe, Arjen Roodselaar, Jan Egil Ruud, John Sanguinetti, Galen Seitz, Salman Sheikh, Mike Shinkarovsky, Rafael Shirakawa, Jeffrey Short, Rodney Sinclair, Steven Slatter, Brian Small, Wilson Snyder, Alex Solomatnikov, Wei Song, Art Stamness, John Stevenson, Patrick Stewart, Rob Stoddard, Todd Strader, John Stroebel, Sven Stucki, Emerson Suguimoto, Gene Sullivan, Renga Sundararajan, Yutetsu Takatsukasa, Peter Tengstrand, Wesley Terpstra, Rui Terra, Stefan Thiede, Gary Thomas, Kevin Thompson, Ian Thompson, Mike Thyer, Hans Tichelaar, Steve Tong, Michael Tresidder, Holger Waechtler, Stefan Wallentowitz, Shawn Wang, Paul Wasson, Greg Waters, Thomas Watts, Eugene Weber, David Welch, Thomas J Whatson, Leon Wildman, Gerald Williams, Trevor Williams, Jeff Winston, Joshua Wise, Clifford Wolf, Johan Wouters, Junyi Xi, Ding Xiaoliang, Jie Xu, Mandy Xu, Luke Yang, and Amir Yazdanbakhsh.

Figure 13: Names on a slide from Wilson Snyder, thanking many partners for their participation in the development of the Verilator simulator (Snyder 2018).

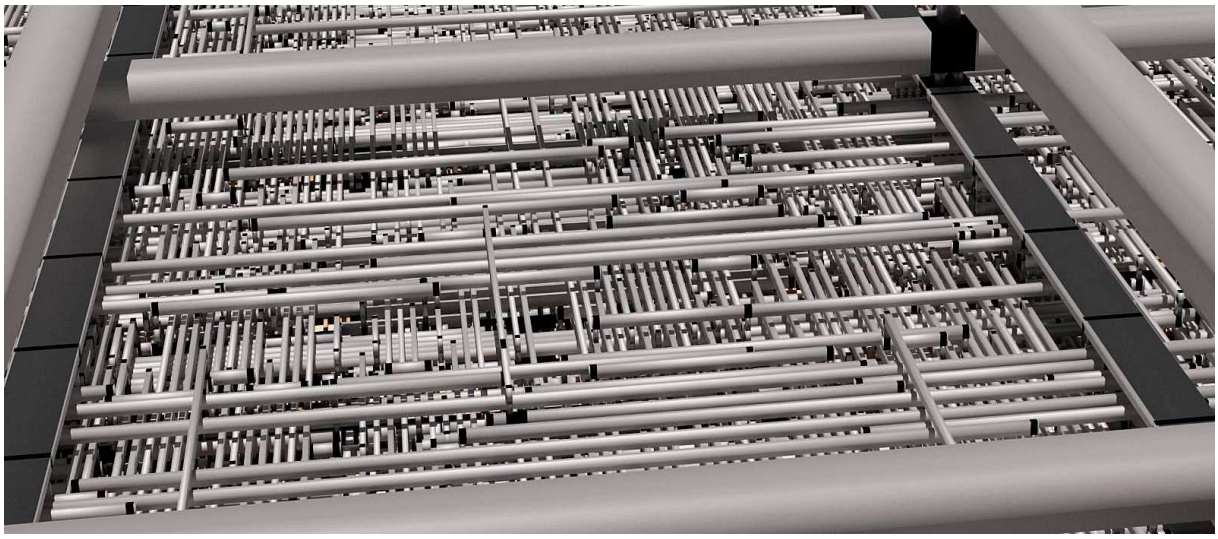


Figure 14: Part of an open RISC-V processor design, generated with OpenLane and the open IHP PDK. The visualization has been produced, for illustrative purposes, using the open 3D computer graphics tool Blender (Schultz/Reith 2025).

Tools can be freely combined to allow for the design of an ASIC within a single day (Venn 2024; OpenLane is an automated flow based on open tools; see Figures 1 and 14). OpenROAD and OpenLane are used to produce GDS II (Graphic Design System) files, which are sent to a fab and used to create photomasks which in turn are used to project structures onto the wafer.

Various organisations and initiatives have subsequently been set up, such as Efabless (which ran out of venture capital in 2025) and the Zero to ASIC Course, for designing and creating chips at a low cost. More initiatives have been springing up since, some of which can partially replace Efabless, including SiliconCompiler.com, Chipfoundry.io, and wafer.space. Cadence has also offered its support to continue chip production (Cadence 2025).

Similar initiatives also been set up elsewhere. The authors have successfully advised the German Federal Ministry of Education and Research to support research on open ASICs, security modules, and PDKs at the German Leibniz Institute IHP, a silicon research institution (cf. our old presentations Reith 2016 and the paper by Weber et al. 2018). Both SkyWater and IHP use 130 nm “legacy node” technology leading to relatively large chips and correspondingly high power consumption, though they have other advantages including a speed of up to 650 GHz (IHP 2025a, 2025b). Note that, in general, larger nodes also have economic significance: TSMC makes about a third of its revenue with technologies of 16 nm or larger and 8% with 130 nm and larger (Shilov 2024). Finally, the Chinese Ministry of Science and Technology also offers significant support for open EDA technologies (cf. Li 2024b; see Fig. 15 for the number of modules needed and Fig. 16 for the objectives).

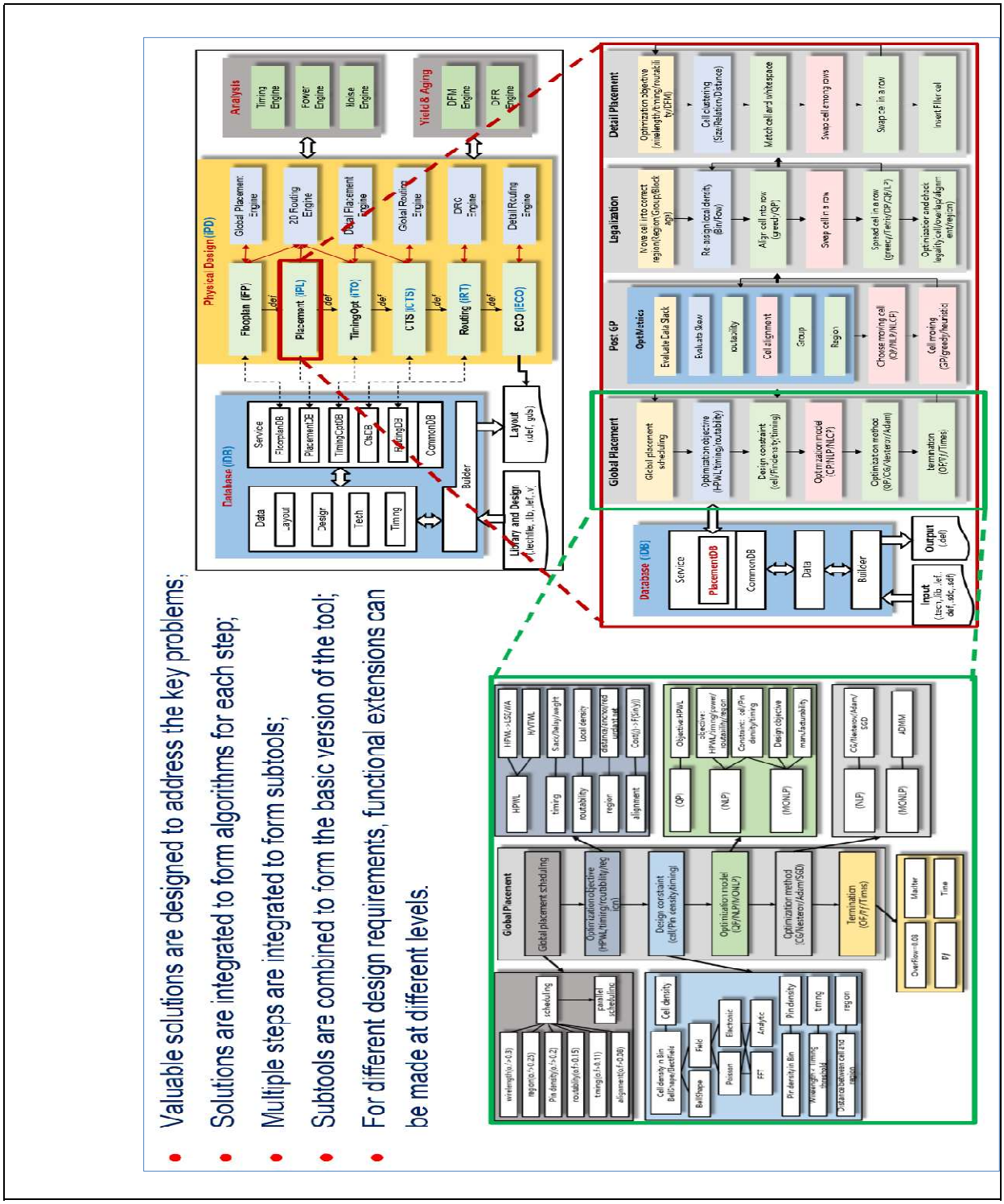


Figure 15: Modules and submodules which need to be integrated in open EDA (Li 2024 b).

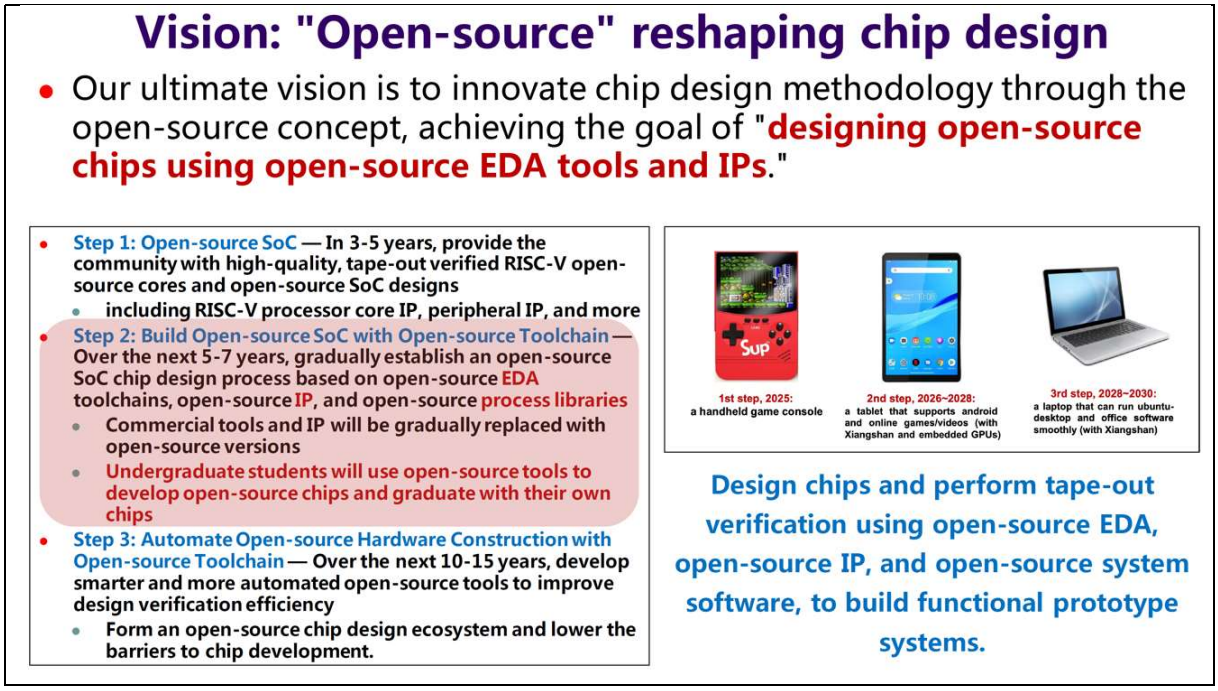


Figure 16: "Commercial tools and IP will be gradually replaced with open-source versions" (Zhao et al. 2025). IP stands for "intellectual property", referring to blocks of code purchased and used. As of writing in 2025, we are not sure whether the plan can be accomplished, but it is certainly ambitious and potentially disruptive (cf. Qiang 2025).

Western companies are already using open tools to reduce the cost of chip design, for cheaper internal prototype development, and to explore new designs not yet possible using legacy software. For example, the use of artificial intelligence instruments cannot be integrated into a proprietary toolflow, as the closed-source software cannot be modified.

Open tools can easily be used inside industry: "We at Infineon are using OpenROAD and OpenLane for more experimental and innovative projects." (Lück et al. 2022)

Using Large Language Models (LLM) to improve designs is a very promising approach to fine-tune chip designs, and open research can help address issues such as that LLMs don't understand the meaning of what they are doing (Kahng 2025).

While it remains to be seen what share of future chips will be produced using the new open chip tools, and which foundries will offer open access, these open components are continuously being improved in terms of features and speed.

The open approach is highly attractive for enthusiasts and students, as well as companies interested in conducting research and developing new products. As Parry of SPHERICAL put it: "The best way to think about this is how Apple designs its iPhones. Instead of using off-the-shelf chips, Apple looks at the entire system's needs and then designs custom microchips to optimise performance. We are applying that same approach to the space industry for the first time, creating microchips that are specifically tailored for satellite electronics." (Parry 2025b).

ChipFlow is an emerging novel type of design house, using the open tool chains and with proprietary PDKs if needed.

For designing ASICs there are still gaps compared to proprietary tools, including in the support of millimetre-wave and high-frequency designs, but these are being addressed, cf. the Design Initiative ("DI") projects supported in Germany, with fabs such as GlobalFoundries and X-FAB and interest from companies such as Cologne Chip and Lubis EDA (BMFTR 2025). Low-cost ASIC production of small designs, primarily for education, has become available, too, as in the Tiny Tapeout project which offers production of an ASIC for just $300 (https://tinytapeout.com/; cf. Fig 17).

There are two or three differences, in total, between the development of open software in general and the development of open EDA tools for ASIC development: one needs to pay for the production in a fab, one needs to wait months for a chip to be produced and packaged, and one needs to sign an NDA for the PDK unless one uses a free and open PDK as are available for somewhat larger or older nodes.

Foundries currently supporting the open approach are SkyWater, IHP, GlobalFoundries (2022) and ICSprout (Zhao et al. 2025). This is not necessarily a growing trend, however, as SkyWater and GlobalFoundries were supported in opening their processes by Google, but the latter has since has reduced its support. As a result, the future is open. The British company Pragmatic, for instance, announced interest in designing open design flexible-substrate chips with open tools (2023), but for production it fell back on legacy tools (Ozer 2024). On the other hand, there are initiatives for open PDKs, as in Japan (https://www.opensusi.org/) as well as groups of users in India such as Riscduino (2025), https://www.vlsisystemdesign.com/, or https://esim.fossee.in/.

Figure 17: Participants producing a tapeout for an ASIC in three hours, as organised by Efabless and Tiny Tapeout (Hackaday Supercon 2024, Stanford; Venn 2024).

Single Tools

Even complex optimisations can take place using open-source tools: the DREAMPlace 4.0 mixed-size placer, originally from the US and subsequently significantly improved in China, is able to improve timing beyond just reducing wire length (Liao 2022, Agnesina et al. 2023; thanks to A. Kahng for pointing to this, cf. Fig. 4). This tool has been used in design flows at Google, Nvidia, and other companies, including for the development of AI accelerators (Lin 2025). Per Nvidia's Agnesina et al. (2023): "Our advances can help the turnaround time of early-stage architectural exploration and assess more accurately and efficiently floorplan modification decisions." Huawei is also conducting research on the same topic (Liao 2022).

DREAMPlace is distributed under a BSD licence, therefore software vendors like Cadence or Synopsys are able to freely integrate it into their products (Lu et al. 2023, Chen et al. 2023). Despite its use, though, the public will most likely never learn about the use of DREAMPlace in the devices they buy. The question oft heard at conferences, "where are the products?", is futile for such modules, just like the number of embedded open RISC-V processors, invisible to end users, which have been said to be shipped in the billions (HPCWire 2024).

Another success story of open design tools is Verilator. This tool simulates circuit designs, sometimes faster than proprietary simulators can manage. It has been open-sourced by DEC and is supported by NXP, Intel, Western Digital, Tesla, Infineon, Shunyao CAD/X-EPIC, and others (Verilator 2025, cf. Fig. 3 and 13). "Verilator is a fast, open source simulator widely used in the ASIC and FPGA ecosystem, offering state-of-the-art (or better) results in contexts otherwise dominated by proprietary offerings." (Antmicro 2022, cf. also the open synthesis tool ABC).

Open tools such as Yosys are already used to program Renesas/Dialog Semiconductor FPGAs (Field Programmable Gate Array chip, cf. Fig. 2, CNX Software 2021, Renesas 2025; see Fig. 18 for the number of open tools).

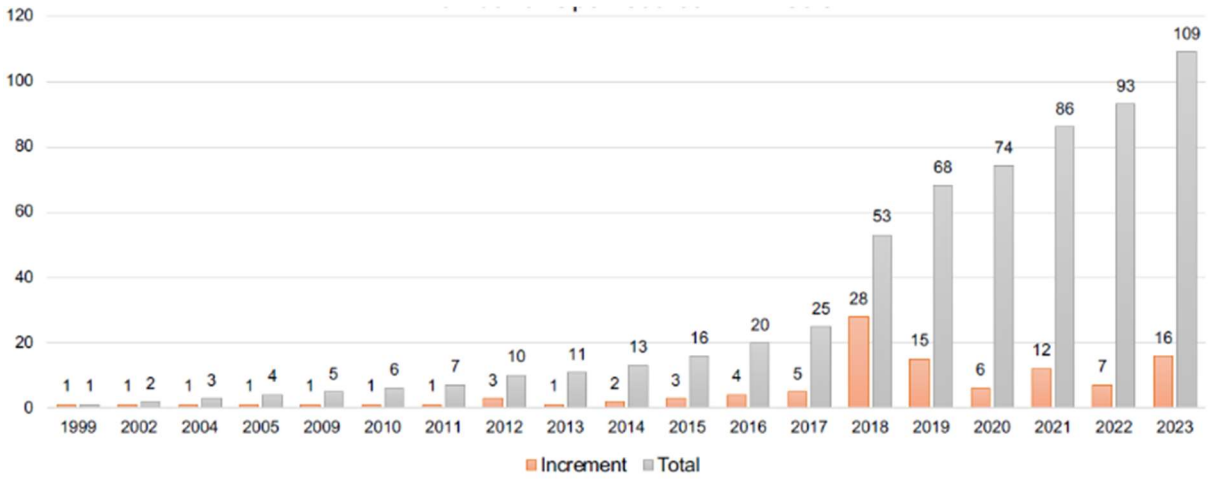


Figure 18: Number of open-source EDA tools, as collected by Li (2024), Beijing Institute of Open Source Chip.

Commercial Activities

Quite a number of companies are exploring the use of the new, open tools and processes, for internal processes, including Google, Infineon, Nvidia, and NXP. Others such as Cadence are supporting it for education. More are exploring it for future use, such as SPHERICAL, Swissbit, Jaguar Land Rover via its investment arm InMotion Ventures, and ChipFlow (see Fig. 19-20).

Figure 19: Companies which have been funding open EDA tools, use them, or are exploring their use, as far as is known to us. A full scan of all open EDA tools documents and research publications into who created them would likely lead to an even larger list (Efabless 2023, Mirhoseini et al. 2025, Rajarathnam et al. 2022, Hammad 2023, Chhabria et al. 2024, Yeshurun 2025, Lück et al. 2022, HEP 2025, ChipFlow 2025b, Kahng 2024, Huang et al. 2022, Chen et al. 2023, imst.de, Verilator 2025, Lubis EDA 2025, Cologne Chip 2025, Wikipedia CC).

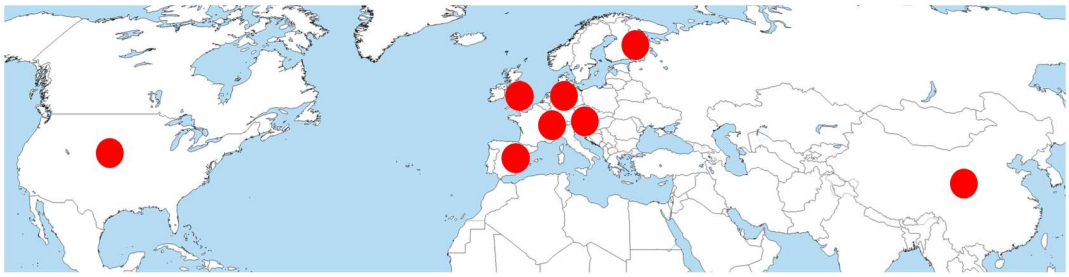


Figure 20: Countries in which open-source developments took place, as mentioned in this paper (source: authors, map based on Wikipedia CC). It would be impossible to trace all the 100+ tools and their improvements, which were referred to in Fig. 18, across borders.

Cost Reduction and Opportunities

With the current proprietary semiconductor production technologies, it is possible to achieve improvements regarding Power consumption, Performance, and Area needed (PPA). The costs of the mainstream EDA software tools, however, are in the five-digit range, per tool, per month, and per workstation. Per company and chip this can sum up to between one and 10 million US Dollars or more. Assuming a use case with many billions in revenue, the costs of EDA tools are not a main cost factor (Venn 2024). For smaller companies, however, which may be producing some novel Internet of Things (IoT) component, a control system for a machine tool, or other task-specific design, this is different. One needs to take costs including tooling into account for profitability, so cheaper tools may increase profitability in particular for lower batch sizes. In this way, open tools could help to facilitate new developments and drive technological innovation.

Free and open tools will also reduce the costs for learning how to use them. For universities price reductions on proprietary software are often available, but students cannot simply explore the tools like any other software, at any time, on their own devices, and neither can curious developers in small companies.

The market for EDA experts is currently relatively small compared to software programmers. If, however, increased technological sovereignty (“chip supremacy”) or deeper innovation is desired, as seen in the EU and in Asia, more students would have to be made interested in working with and on EDA software. For somebody targeting the latest and most powerful semiconductor technology the current proprietary tools practically guarantee the success of production from end-to-end, though. But recall the Chinese ambitions to replace “commercial tools and IP” with open-source versions.

Security: Openness and Formal Verification

The openness of tools and components is a prerequisite of security for a party relying on the correctness of a system, as otherwise it does not know precisely what is being used (Kerckhoffs 1883, Thompson 1984). In traditional chip design so-called Intellectual Property (IP) components are used, which may not be trustworthy and cannot be inspected, as with proprietary components for a military Global Positioning System (GPS) receiver (Coleman 2023). Moreover, the mainstream tools themselves may contain Trojan horses, as with known attacks including Stuxnet (Kushner 2013) or the attack on the SolarWinds Orion software which was traced back to programmers in Belarus (New York Times 2021).

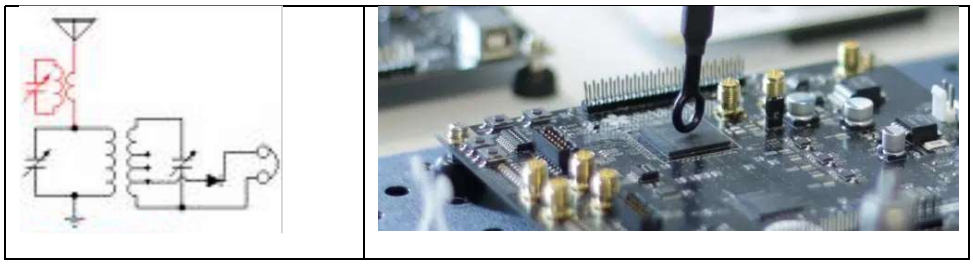
With an open approach cryptographically relevant components such as random number generators can be built in a way which makes them observable and auditable. Per Schneier, 2007: “Break the random-number generator, and most of the time you break the entire security system.” As one example, it was once discussed whether a backdoor had been inserted into a US National Institute of Standards and Technology (NIST) standard (cf. Shumow/Ferguson 2007). A random number generator should therefore be designed, validated, and improved through a visible community-driven process. It is even possible to

create open-source protections against hardware tampering, i.e. shielding against physical probes (Ngo et al. 2017; cf. IHP 2024 describing research on an open random number generator for Caliptra).

With the open approach, components can have special security-related features, as with the proprietary approach, but now with the benefit of full transparency. As Grawunder of Swissbit put it: “Currently, we […] have to buy crypto algorithms under closed source […] Our position is that security in particular thrives on being verified, understood, and tested by a broad community, and on having a common standing about the value of the methods implemented there.” (Grawunder 2022).

An open component may be mathematically proven to be free of vulnerabilities. It can, for example, be formally proven that a processor only executes the commands it is supposed to execute according to its instruction set architecture (ISA) (Henkes et al. 2024).

To implement such special security features properly the EDA tool should cooperate and not optimise anything away. As Guilley put it: “Formal specifications, open-source designs, and EDA shall interoperate gracefully to ensure the expected function. For this vision to become reality, we need to enable protection at scale, whilst allowing for knowledge sharing.” (Guilley 2024).



Figures 21 and 22: Demonstration of a security risk in closed products, here a resonating circuit and an antenna are added during production, to function as a Trojan horse (Tehranipoor 2024); probing for the extraction of a secret key (Secure-IC 2025).

In one research project our partners implemented exactly that approach: a hardware description language, namely SpinalHDL, was modified to support a method of protecting against side-channel attacks (Henkes et al. 2024, Buschkowski et al. 2023; cf. Figures 21 and 22).

In practice any “secure” implementation should be produced in a secure environment and formally proven, or at least thoroughly evaluated by several teams; it may also be formally certified where required.

The concept of open, verified ASICs could be extended to the operating system and its applications, with segregation allowing for the use of new, confidential components, as well as for large or legacy applications.

As to chip production itself, security could be enhanced if several identical fabrication facilities allowed for a free choice of where a chip is produced, as discussed above, and if

automatic analysis (“de-gating” to identify all transistor gates) of chips were supported to verify their contents. We do not delve into the latter options here, which would require demand and considerable research and development (for details, see Weber et al. 2023, Weber et al. 2024, and Cyberagentur 2025).

Options for Future Fabs

To show the scope of potential future change using the paradigm of openness, we mention the following options:

- Open mask production is one option (Xyalis in France, cf. Morey-Chaisemartin 2024).
- Another option to be considered is the creation of transparent, standard fabs. These would be transparent in the sense that their PDKs, equipment configurations, and process recipes are open and freely available. They may or may not be considered as “Trusted Fabs.” These open fabs could be standardised in the sense that multiple copies of the facilities could be set up in different regions and countries. Such standardisation could lead to further cost reductions as economies of scale can lower the price of consumables and tools (cf. Herfurth et al. 2025).
- The scaling-down of fabs is under investigation, too, with the relatively cheap Japanese ICPS Minimal Fab (Yokogawa 2024).
- Larger chip structures are being considered among enthusiasts as well, to ease production and later inspection of chips (LibreSilicon 2025).

Summary Regarding Innovation

A number of companies have already identified new fields in which free and open EDA components can reduce costs. Furthermore, the open approach enables new and unexpected research and development paths, faster and more favourable reactions to errors, and a wide dissemination of knowledge.

To provide an example, the authors have been active regarding security modules: we have obtained interest from industry for the research projects *Hardening the Value Chain Through Open Source, Trustworthy EDA Tools and Processors (HEP)* and *SIGN-HEP*, abbreviated by the German Federal Ministry of Education and Research as VE-HEP and DI-SIGN-HEP, with DI standing for Design Initiative. These projects are affiliated with the following industry partners: Bosch, Elektrobit, Hensoldt Cyber, IAV, Nitrokey, Swissbit/Hyperstone, Volkswagen/Cariad, and Secure-IC, conducting research on an open Caliptra-compliant hardware security module (cf. IHP 2024, RISC-V International 2023, https://hep-alliance.org/). From this example one can see that open EDA is not simply a trend but that it depends on active individuals.

Furthermore, innovation is meandering: some appear to have reduced their interest, such as Google and Efabless, while others increased their interest, like the Chinese iEDA initiative, Cadence for taking over some of the Efabless business, and users of Verilator or DREAMPlace.

In sum, open chip designs, open EDA, and open PDKs have the potential to reduce development costs, to lead to process innovations, improve security, and can help to alleviate the skills shortage. Overall, this can lead to increased profitability. The quality of the open components may not yet always reach that of closed options, but this may change. Current community-building in the US, Europe, and China is increasing (cf. Li 2024b, Kahng 2024 and Venn 2024).

Key innovations in the process of emerging can be summarised as follows:

1. An easy-to-use and low-cost competitor to the EDA oligopoly is emerging. Some tools are already used for commercial products, while the usability of entirely open tool chains is being explored. Furthermore, open tools are actively used by individuals, students, educators, and by in-house development teams.
2. Singular open components are already being used for the design of AI-related chips.
3. The components for open EDA are being developed, shared, and improved across the globe, by companies, research institutions, and individuals, and even integrated into proprietary tools.
4. Simple ASICs can already be produced very cheaply without the need to sign an NDA.
5. Lower-cost ASIC design services are emerging for those companies who do not want to learn how to use the new tools themselves.
6. If powerful small-node technology is made unreachable for some countries, these countries will instead search for similarly energy-efficient technologies which may turn out to be cheaper.
7. The security of all such designs is increased in so far as they are open and thus observable and auditable.
8. Free and open mathematically provably correct hardware components have already emerged, including formally ISA-compliant processors and protections against side-channel attacks, which randomise signals which might be eavesdropped.
9. More secure components can contribute to more secure supply chains, and be combined with open or Trusted Fabs, formally proven operating systems, and even run side-by-side with non-verified hardware and applications.

All of this is beginning to reduce costs, increase competition, ease innovation, and improve security. Finally, improved accessibility to tools means more students and enthusiasts have already become interested in hardware design.

Unstoppable Ecosystems and Components

The process towards open-source EDA faces difficulties, but can be fairly judged to be unstoppable and irreversible (using words by Andrew Kahng 2024b). Chip purchasers may, in the future, demand open access to chip designs, EDA processes, and PDKs. Providers of open EDA tools may need to offer support for professional users, as is available for companies using Linux. Such open EDA tools may also be used with proprietary PDKs; foundries with

surplus capacity or who want to reduce costs for their customers, on the other hand, may choose to open their PDKs. The availability of open PDKs for smaller and more advanced node sizes will be an important factor influencing the market share of open-source tools in EDA (similarly: Nebel/Weigel 2025).

A possible issue is whether emerging, purportedly consumer-protecting, EU regulation, such as the Cyber Resilience Act, will lead to higher burdens on EU-based providers of open hardware components than the burdens US and Chinese producers will experience. In the EU, the open hardware providers may need to certify their output if they provide paid services, e.g. for hardware components which are security-relevant.

The current main routes forward for the open-source community are:

- Aim at production-grade designs. This means to create a competitor to the Big Three incumbent tool providers, or to let them integrate new components.
- Develop towards open designs to be sent to a fab, or have confidential PDKs to be used only after signing an NDA. As of writing, SkyWater, IHP, GlobalFoundries and ICSprout support the open approach (cf. Zhao et al. 2025).
- Restrict oneself to supporting education only. This is still valuable, and Synopsys and Cadence have been exploring this path. Cheap ASICs would only be produced to allow students to experience success, rather than at volume for commercial use.
- Mix and merge the open and proprietary components in various ways, as has been done by Google, Nvidia, NXP, and others.

In any case, the issue comes up whether to cooperate or to compete: this is a central dilemma for open-source EDA development. To continue to bring open-source EDA tools to a level suitable for production-grade designs, two fundamental approaches exist:

a) Coordinated global development efforts; or
b) Decentralised, parallel development by independent players.

At first glance coordinated development appears to be the more efficient path, promising faster progress and better use of resources. However, large-scale collaborations often face bureaucratic overhead, diffuse funding priorities, and a loss of the agile, modular spirit that defines many successful open-source projects. The effort required for coordination can be substantial, and may even slow progress if not managed well.

In contrast, decentralised competition encourages innovation and allows teams to pursue solutions that are tailored to regional or application-specific needs. It maintains the open-source ethos of experimentation and flexibility, but this approach risks duplication of effort, slower overall progress, and fragmentation.

"The commercial tools are extremely sophisticated and advanced. It's pointless to try catching up, esp. with open-source."

→ Essential components of the commercial tool chain were once university projects.
→ The tools consist of code, no magic involved (pun intended).
→ The more wheels exist, the easier it becomes to invent new ones.
→ Not advanced: No browser interfaces, no Python libraries, no CI/CD platforms, no AI/ML interfaces, etc.
→ Commercial EDA tools rarely hang out with modern software technology

Figure 23: Arguments pro and contra open EDA tools, as expressed by a project management organisation working on behalf of the German Federal Ministry of Research, Technology, and Space (from a slide of Schreiber, Tauchnitz 2024).

The duplication of work on OpenROAD, iEDA, and on Coriolis, for example, may lead to lower costs because of competition, but also to a waste of resources. The essentially US-based OpenROAD and OpenLane may be updated internationally, or, alternatively, the French Coriolis toolchain could be brought to practical usability (cf. FOSSi Foundation 2024). Such competing schemes, partially built out of the same components, might coexist just as with the numerous variants of Linux-based operating systems available today.

Both strategies come with benefits and trade-offs, and it is difficult to take a decision. We tend to think that, as so much needs to be improved and that the situation is still fragile with no ubiquitous commercial support, worldwide cooperation might be the best path forward. Furthermore, transborder cooperation is a fact, and one should not exclude any entity working on generating innovative or secure components to protect their independence and the sovereignty of their country, as seen in China.

Governmental support may be needed and justifiable for the production of formally proven tools and components. These would, initially, be valuable for critical infrastructures and the armed forces, and could then be released as dual-use components in all world regions. Formally-proven components are key to achieving secured value chains (Weber et al. 2023).

The formation of a formal organisation, or several distinct organisations, might help, provided it does not prevent re-use of new components in other regions and works efficiently. This could take the form of a foundation (cf. Kahng 2024) like the Open Compute Project Foundation, the Linux Foundation, or the RISC-V Foundation (cf. OCP 2024). If needed, such an organisation should be based in a neutral country which does not impose export restrictions on security-relevant components.

Outlook

In summary, several paths have become visible:

- Open EDA could essentially be used for education, not for production. Some open PDKs would be used for testing to build a real ASIC.
- A competitor to the Big Three could be created. For products, it may well be used with closed PDKs.
- Customers could demand PDKs for more powerful technologies to be made available without NDAs, or fabs could offer them in competition.
- Highly secure EDA processes could be developed, with full transparency and verification up to the level of formal proofs of correctness.
- Innovative modules could be used within either open or proprietary tool chains, improving efficiency or security.

What could that mean in the short term? Some options for investors and governments are:

For investors:

- Use the new open approaches, just as many already do (cf. Fig, 1-10, Fig. 19), to get acquainted with them for internal learning, for research, to look out for cost reduction opportunities, and to educate potential applicants.
- Explore using the tools for products, like Google, Nvidia, NXP, Huawei, and InMotion are doing.
- Communicate that an open, free competitor could be useful to reduce prices, ease innovation, and increase security.
- Cooperate to improve the tools, as with a cost-sharing organisation like CHIPS Alliance or the Linux Foundation which have already demonstrated that the approach can work. New groups in formation include the US OpenROAD, Chinese iEDA, the emerging EU Chips Design Platform (EuroCDP 2025), and the HEP-Alliance.
- If security plays a large role in a business, consider the use or development of open and formally proven components throughout the entire value chain.

For governments:

- Explore global cooperation with China, India, and more; produce international, comparative analyses of strengths and deficits; develop plans for cost sharing and free use, and implement them.
- Don’t get discouraged by those who claim the open approach will never be as usable as the proprietary tools from the Big Three (cf. Fig. 23). While unprovable, that may be correct, particularly for the latest high-tech small process nodes, but beyond that the chips produced with open methods and somewhat larger nodes do run and processes and results will only improve.
- Support open EDA, PDKs, and fabs by funding or otherwise enabling and encouraging research, the formation of foundations and agencies etc., and in procurement.

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