THE EUROPEAN REFERENCE FAB

Blueprint for a Trusted and Transparent Manufacturing Network

Exposé:

The Transparent Reference Fab (TRF) is a modular 300-mm blueprint (130 → 65 nm, Packaging-First) with open PDKs, auditable processes, and a Comply-to-Connect label. It scales as a network of clonable fabs, monetises via trusted-premium and advanced-packaging services, and remains voluntary and EU-law compliant in its co-operation. Tranche-based financing links disbursements to milestones (construction/tool IQ/OQ, PDK/MPW, audit go-live, 65-nm release); governance options (PPP, SPV, foundation; private with a public-service mandate) remain open. Phase 0 validates site, CAPEX/OPEX corridors, demand anchors (LTAs/Take-or-Pay), and the RefFab Academy. Recommendation: establish an EU task force within 6–12 months to pilot; in parallel, industry MoUs for MPW and a packaging pilot.
All figures are corridors; validation occurs in Phase 0.

Packaging-First. Trusted by Design.

Norbert Herfurth; Arnd Weber; Steffen Reith; Anna Herfurth; Rene Scholz; Torsten Grawunder
ref-fab@hep-alliance.org

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Transparent Reference Fab for Europe: Open, scalable semiconductor manufacturing as a strategic concept

Executive Summary

Europe faces, in 2025, the existential task of strengthening its technological sovereignty in semiconductor manufacturing. The European Chips Act of 2022 set the goal of increasing Europe's share of global chip fabrication by 2030 from under 10% to 20%—an ambitious undertaking intended to mobilise a total of around 43 bn € in investment[1]. Meanwhile, all 27 EU Member States, under a Semicon Coalition, are calling for an evolution towards a "Chips Act 2.0". Rather than focusing on market share alone, this aims to close critical gaps: secure key technologies, accelerate permitting procedures, and deepen competencies along the entire microelectronics value chain[2]. In parallel, the EU Agency for Cybersecurity (ENISA) warns of increasing cyberattacks on critical infrastructures—a wake-up call that trustworthy, auditable hardware has become a security imperative. Worldwide, other industrial nations are pushing ahead with semiconductor expansion: Japan is investing billions in the Rapidus initiative (target: 2-nm mass production by 2027)[3], and the United States launched the CHIPS and Science Act (52 bn $), followed by major investments such as Texas Instruments' plan exceeding 60 bn $ for new fabs in Texas and Utah[4,5]. China, too, has been flooding the sector with subsidies for years to build domestic fabs. Within Europe, there are isolated initiatives—e.g., Ireland's "Silicon Island" strategy (national semiconductor offensive since 2025)[6], the Swiss "Chip FabLab" project co-led by ETH Zurich[7], or plans around CSIC/CNM in Spain. These individual efforts matter but, lacking critical mass, cannot solve the root problem. Europe must consolidate its strategy and act as one to be prepared against geopolitical risks, supply bottlenecks, and

[1] https://commission.europa.eu/strategy-and-policy/priorities-2019-2024/europe-fit-digital-age/european-chips-act_en

[2] https://digital-strategy.ec.europa.eu/en/news/semicon-coalition-calls-reinforced-chips-act

[3] https://www.rapidus.inc/en/tech/te0006

[4] https://bidenwhitehouse.archives.gov/briefing-room/statements-releases/2022/08/09/fact-sheet-chips-and-science-act-will-lower-costs-create-jobs-strengthen-supply-chains-and-counter-china

[5] https://www.ti.com/about-ti/newsroom/news-releases/2025/texas-instruments-plans-to-invest-more-than--60-billion-to-manufacture-billions-of-foundational-semiconductors-in-the-us.html

[6] https://enterprise.gov.ie/en/publications/silicon-island-a-national-semiconductor-strategy.html

[7] https://ee.ethz.ch/news-and-events/d-itet-news-channel/2025/08/boosting-swiss-semiconductors-plans-for-chip-factory-gain-media-attention.html

technological lag. Against this background, this paper presents the concept of a Transparent Reference Fab as a proactive response.

The Transparent Reference Fab for Europe is a proposed reference semiconductor plant designed to be open, scalable, and production-ready. It serves as an open-source blueprint for the rapid build-out of additional fabs in Europe. Core principles of this approach are:

• **Series-capable manufacturing model instead of a pilot line:** Unlike typical pilot lines (which often have a demonstration character and, at best, capacities for small-series production), the Reference Fab is designed from the outset for industrial volumes and 24/7 operation. It is intended to shoulder real production loads and operate economically, so that any plant copied from this model is production-ready from day one and does not require a costly transition from pilot to series production.

• **Transparent open-source blueprint:** All key processes, equipment parameters, and fab operations are, in principle, openly documented and made accessible for re-use. This transparency allows European industrial actors and states to use the fab as a blueprint to build new plants autonomously with lower development risk. It also creates trust in the chips produced: security-relevant semiconductors can be examined down to the process level, ensuring trusted electronics “Made in Europe”. Any backdoors or manipulations are significantly harder to conceal in a transparent manufacturing process. **Open-PDK & open-source EDA:** Based on open PDKs and reproducible, auditable toolflows (CI/CD), reference IPs and assembly design kits are provided; this measurably lowers entry barriers and audit times. The project thus aims for the **“Trusted EU Fab Network”** label—independent bodies should **certify the trustworthiness** of production on the basis of the open documentation and inspections.

• **Packaging-First & chiplet-readiness:** Performance, energy, reliability, and security targets are now decided in the back end/SiP/SoP. Therefore, advanced packaging is a core component from day 1: RDL/fan-out, interposer/2.5D, and co-packaging of leading-edge compute dies with 65-nm periphery (PMIC, mixed-signal, sensor IF). We anchor chiplet standards (e.g., UCIe/BoW/OpenHBI), design-for-packaging, and qualified test flows (KGD→SLT). In this way, we do not widen the gap to the leading edge but bridge it systemically. Close exchange with EU-funded pilot lines (e.g., APECS) is required here.

• **Focus on 65-nm CMOS as a strategic technology node:** The Reference Fab targets the established 65-nm node, as it is future-proof and sufficiently performant for many critical applications. Sectors such as automotive, industrial, med-tech and aerospace can manufacture their microcontrollers, ASICs and mixed-signal components at 65 nm—robustly, cost-effectively, and in high volumes. Forecasts indicate that even after 2030, a significant share of global chip demand will fall to technologies ≥65 nm (especially analogue/power electronic chips), while <10 nm accounts for only ~12%. As a bridging technology, operations will initially start on the proven 130-nm node, for which equipment and open process data and PDKs are immediately available in Europe. This bridging approach enables a rapid start of production with high yield, while the 65-nm line is ramped

in parallel to maturity. The fab infrastructure is designed modularly so that a later upgrade to 65 nm (or smaller) is possible without fundamental replanning. The focus initially remains on 65 nm as the “sweet spot” between maturity, availability, and sovereignty gains. Importantly, selected platforms will be assured long-term availability (target corridor ≥ 15 years) with obsolescence pathways; certification and qualification pathways (e.g., AEC-Q100/IEC 61508/DO-254) are part of the offering. This explicitly avoids a commodity-volume model and instead pursues a trusted-premium approach with service and quality premiums.

• **Data-driven manufacturing, audit trails & automation:** Dense inline metrology, SPC/ML-assisted control, and end-to-end feedback from front-/back-end data shorten ramp-ups and create verifiable quality and trust metrics; this also includes robotics-based automation processes. Where sensible, selective single-wafer steps are used; furnace/batch processes remain economical.

• **Use of existing resources and expertise:** The Reference Fab should be located in close physical proximity to existing research and pilot lines such as IHP, CEA-Leti, or imec in order to translate existing process know-how directly into industrial implementation. This proximity enables a significantly accelerated ramp-up, as established teams, qualified equipment, and proven process modules can be used directly. At the same time, the Reference Fab remains institutionally independent—it is not an extension of a research institution but an industrial Reference Fab with its own mandate. By purposefully integrating research know-how into an open production model, Europe can become operational more quickly without starting from zero.

• **Governance & public-trust mandate (PPP):** Public ownership or a public-trust mandate—institutionally independent of R&D institutions, with physical proximity/co-location; non-discrimination, open audit interfaces (traceability down to lot/wafer level), clear access rules; industry co-investments in equipment/packaging. This ensures replicability, planability, and verifiable trust mechanisms.

• **Talent, training & trusted personnel (RefFab Academy):** The Reference Fab embeds qualification as a core task. The RefFab Academy provides core curricula, EQF-aligned micro-credentials, and a Skills-Passport directly linked to RBAC/Comply-to-Connect in the MES. Packaging-First (SiP/UCIe, RDL/fan-out, ATE/SLT) starts on day 1; training is delivered via standardised Learning Cells and a “learning-workshop-in-a-box” (on-/off-the-job, bootcamps, VR/AR, digital twin). Dual/VET and higher-education pathways are connected via MoUs to existing programmes; rotations (fab/OSAT/R&I) shorten time-to-competence. Active recruiting (EU programmes, reskilling, international hiring) is flanked by family-ready offers (shift-compatible childcare, language tracks, mentoring; Just-Culture). GDPR-compliant, risk-based background checks and a compliance gate (antitrust/FDI/dual-use/IP/privacy) safeguard publications and artefacts. Open PDKs/EDA and freely available ADKs plus MPWs remain the instructional foundation. Target corridor per Reference Fab in the build-up phase: 30–50 engineers and 70–120 technicians/operators p.a.; long term: ~20 and ~60 p.a., respectively (site-specific validation in Phase 0).

• **Scalable reference solution & network concept:** The overarching goal is a multiplicative effect: the Reference Fab serves as a blueprint that can be copied one-to-one and rolled out across several European regions. Each new fab built to this model immediately increases regional manufacturing capacity and supply-chain resilience. By standardising the architecture, even production lots and personnel can be exchanged between sites. If a fab fails in a crisis situation, others with identical equipment can temporarily step in—improving supply security. Such a network of identical, trustworthy fabs would reduce Europe's dependence on non-European suppliers while also serving as a platform for innovation (e.g., joint further development of new process modules, open IP libraries).

• **Specialisation for niche products:** Multiple fabs with an identical CMOS base can purposefully differentiate themselves through process-modular add-ons (e.g., RF, power, sensor modules, photonics)—without changing the base technology. In this way, we combine economies of scale with technological differentiation in higher-margin niches. The result is a flexible manufacturing ecosystem that promotes both innovation and specialisation in niche markets.

• **Demand anchors:** Public procurement (critical infrastructure/public administration/security) secures base load; industry co-investments lift packaging/test capacities. Delineation: no EUV/leading-edge foundry, no commodity volume model—focus on trusted-premium, SiP/chiplets, and long product life cycles.

• **Financing & economic viability (brief overview):** PPP structure with public base load and industry co-investments; subsidised share of CAPEX (site/EU programmes); staged funding tied to milestones (MPW start, 65-nm ramp, packaging pilot); revenue mix: foundry, packaging/test, services (MPW, certification, obsolescence management).

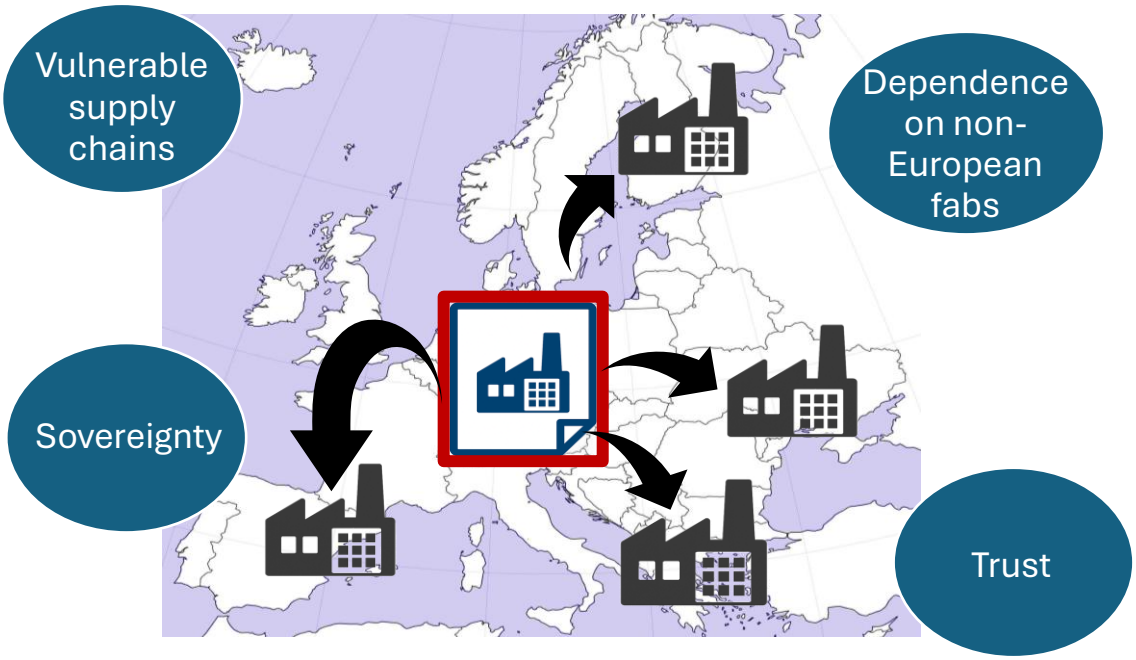
• **Guardrails (without hard promises):** MPW ≥ 4/year (130 nm) & ≥ 2/year (65 nm), SiP-MPW from Year 2; packaging targets: RDL pitch 10 → ≤ 5 µm, microbump ≤ 55 µm; long-term supply ≥ 15 years; trust KPIs: published yield/DPPM & traceability metrics.

Perspective 2040+: The relevance of ≥ 65-nm classes will persist well beyond the 2030s due to analogue/mixed-signal content, power electronics, eNVM MCUs, RF front-ends, rad-hard/space electronics, and security requirements. Long-lifecycle industries (automotive/automation/med-tech/aerospace) and chiplet architectures further stabilise demand: 65 nm takes on peripheral functions, sensing, PMIC, safety MCU, while leading-edge compute is integrated via co-packaging. The network can—where sensible—shrink modularly or expand its SiP/OSAT footprint without changing the business model.

This Executive Summary addresses policymakers at EU and national level as well as potential funders in public administration and industry. It outlines, in compact form, the vision of a Transparent Reference Fab and its benefits. The recommendation is to advance this strategic concept swiftly with political backing and initial funding. In view of the ongoing reform efforts around the Chips Act, the heightened threat environment, and global

investment dynamics, now is the right moment to lay the foundations for open and sovereign semiconductor manufacturing in Europe.

Note (disclaimer): This paper presents a concept and sketches initial proposals for implementation and financing. Delivering a robust realisation will require deeper analysis and a detailed execution plan. Developing these is an integral part of the concept and the subject of Phase 0.



Assumptions, Scope & Non-Goals

- This paper proposes a **replicable Reference Fab blueprint** (capabilities, governance, training) — **not** a site decision or investment commitment.
- Core focus: **packaging-first** (SiP/RDL/Fan-Out), **test/ATE/SLT**, open PDK/EDA integration, **auditability**, and **workforce** pipelines.
- Technology path: **130 → 65 nm** as *evergreen* nodes for AMS/MCU/PMIC/RF/IoT; concrete volumes/product mixes are **partner-specific**.
- Complementary to leading-edge fabs; aims at **resilience, qualification, and SME access**, not volume competition.
- Implementation is **phase-gated** (Phase-0 → Go/No-Go) with measurable milestones.
- Quantitative ranges are **scenario-based**; all figures are indicative pending partner due diligence.

About the Authors:

Norbert Herfurth earned his PhD (TU Berlin, 2020) in semiconductor failure analysis. 2013–2019 he worked in TU Berlin's Semiconductor Devices group. Since 2020 at IHP—initially as cross-department postdoc/project coordinator, now research group lead. He initiated and still shapes IHP's open-source activities (especially open source hardware and chiplet integration), including Europe's first open-source PDK.

Current employment is for identification only; views are personal.
Contact: ref-fab@hep-alliance.org

Arnd Weber is an economist and sociologist. Until retirement he was researcher at KIT, advising the EU Commission, EU Parliament and German government. His PhD traced the rise of public-key cryptography; he co-designed untraceable, loss-tolerant e-money, analysed the Dresden semiconductor cluster, and in 2003 predicted issues in European mobile data services. He founded "Quattro S" and helped initiate the HEP project on an open hardware security module. Currently he is subcontractor to IHP for the SIGN-HEP project (information is for identification only; views are personal). Contact: arnd.weber@alumni.kit.edu

Steffen Reith is Professor of Theoretical Computer Science at RheinMain University of Applied Sciences in Wiesbaden. During his work at Elektrobit Automotive, he developed products with cryptographic functions for use in current automobiles.

Contact: Steffen.Reith@hs-rm.de

Anna Herfurth is Head of Human Resources at IHP. She brings over six years of leadership experience in strategic HR, organizational development, and digital transformation. At IHP, she drives talent development, employer branding, and workforce structures for a high-tech research environment. In the Reference Fab initiative, she contributes expertise in HR strategy, skills pipelines, and dual education models for the semiconductor industry.

Current employment is for identification only; views are personal.

René Scholz earned a PhD in physics (MLU Halle-Wittenberg, 1999) after research on point-defect diffusion in Si and GaAs at the Max Planck Institute of Microstructure Physics. He joined IHP in 2001 for RF characterization and modeling, later leading the MPW Service and PDK development. He also holds an MBA (European University Viadrina, 2008). Recently, he contributes to IHP's open-source BiCMOS PDK.

Current employment is for identification only; views are personal.
www.linkedin.com/in/rene-scholz-86b4473

Torsten Grawunder is a hardware/security engineer. He studied physics of electronic components at TU Chemnitz, specializing in ASIC design for communication technology. Since 2021 he has worked at Swissbit Germany AG in system design/embedded solutions (APATS), creating and analyzing pre-development system concepts for future NAND-flash products and coordinating Swissbit's funding processes. Previously, for 20+ years, he developed encryption hardware for ISDN, ATM and Ethernet at Biodata, secunet and Rohde & Schwarz SIT.

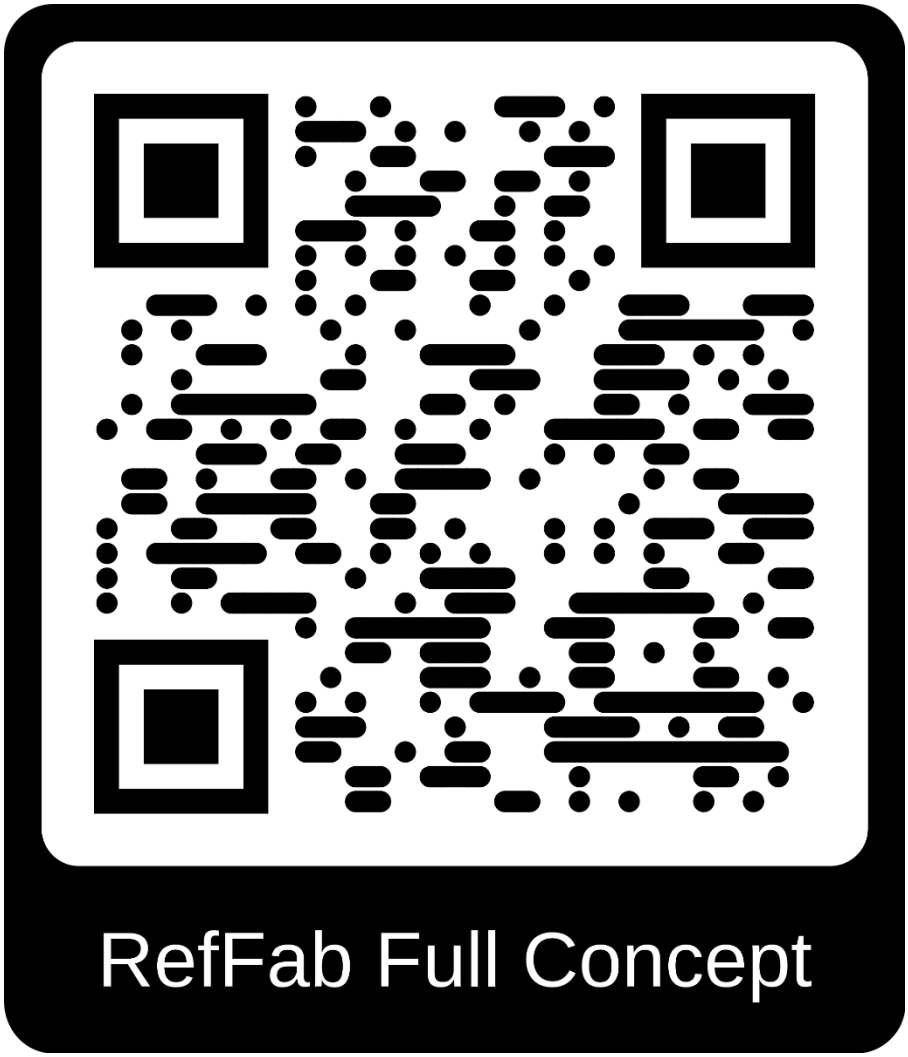
Contact: torsten.grawunder@swissbit.com

List of Abbreviations (Executive Summary)

Abbreviation	Meaning
ADK	Assembly Design Kit
AMS	Analogue and Mixed-Signal
ATE	Automated Test Equipment
CAPEX	Capital Expenditure
CD/CI	Continuous Deployment / Continuous Integration
ENISA	European Union Agency for Cybersecurity
EQF	European Qualifications Framework
FDI	Foreign Direct Investment
IP	Intellectual Property
IQ/OQ	Installation Qualification / Operational Qualification
KRITIS	Critical Infrastructure (German: *Kritische Infrastrukturen*)
LTAs	Long-Term Agreements
MES	Manufacturing Execution System
ML	Machine Learning
MoU	Memorandum of Understanding
MPW	Multi-Project Wafer
OPEX	Operational Expenditure
OSAT	Outsourced Semiconductor Assembly and Test
PDK	Process Design Kit
PMIC	Power Management Integrated Circuit
PPP	Public–Private Partnership
RBAC	Role-Based Access Control
RDL	Redistribution Layer
SiP	System-in-Package
SLT	System-Level Test
SoC	System-on-Chip
SoP	System-on-Package
SPC	Statistical Process Control
SPV	Special Purpose Vehicle
TRF	Transparent Reference Fab
UCIe	Universal Chiplet Interconnect Express
VET	Vocational Education and Training
WSPM	Wafer Starts per Month

Further Information

Landing page & downloads: www.hep-alliance.org/Reference-Fab
(QR code resolves to this page)



Contact & briefing requests: ref-fab@hep-alliance.org
(or: nor.herfurth@gmail.com)

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